



WHITE PAPER

Limitations of 2D x-ray inspection

What you will learn in this technical paper:

- What level of x-ray inspection is needed on different components
- How laminography separates layers on double-sided components, and evaluates solder presence
- Void calculation on multilayer, double-sided boards
- Determining the actual fill level of THT components
- Time saving failure analysis of BGA's; micro3Dslice vs CT scan

Inspection techniques for Electronic components

While x-ray inspection of electronics has existed for several decades, the continuous shift in electronics design and manufacturing to smaller, more dense products, is driving x-ray technology forward. In the 55 years since Gordon Moore suggested that the number of components in an integrated circuit (IC) would double every year, the challenge to design, build, and test those electronics has grown as well.

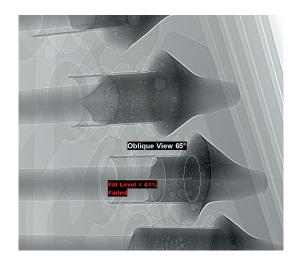




For single-sided or lower component-density circuit boards, traditional 2D microfocus x-ray imaging provides a very useful image that can be interpreted by operators and software algorithms into a Pass/Fail state. With the right system and technique, a trained operator can achieve very high contrast and high resolution. A good quality image [BGA (ball grid array) in Figure 1] enables the operator or a software program to then qualify solder joints depending on the criteria that are often determined by the end-use of the product. These criteria for the quality of solder joints are usually classified into IPC (Institute for Printed Circuits) classes, such as 1, 2, and 3. These classes of workmanship help a customer to decide what level of inspection is needed, and what thresholds need to be in place for optical and x-ray inspection systems. Components with "hidden" solder joints are the ones that typically require x-ray inspection.

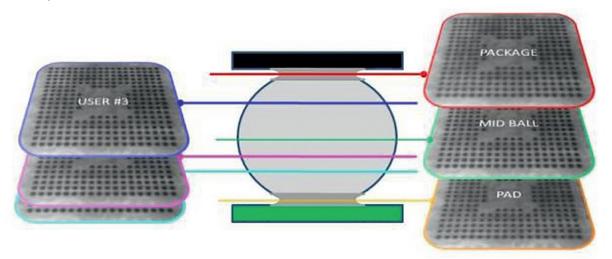
These include, but aren't limited to: BGAs, PTHs (plated through hole components, Figure 2), LGAs (land grid arrays), CGAs (column grid arrays), and QFNs (quad flat no-leads). These components have solder connections that are not visible or inspectable on the surface of the board. Depending on the class of workmanship required, these often mandate x-ray inspection. While a simple high-resolution x-ray image often provides enough information to process a Pass/Fail decision, quite often the high-density "double-sidedness" of modern circuitry prevents this.





Laminography to Visualize layers

This challenge led the inspection industry to an x-ray technology that allows the user to separate top from bottom layers. By checking these layers, one could evaluate the presence of solder in a single or several planes (Figure 3), thereby estimating the overall volume of solder based on those individual "planes." While this definition of "laminography" has historically been successfully used in production and able to maintain line speeds, newer laminography techniques allow reconstruction of the entire volume of a component on a PCB (printed circuit board) in the same amount of time.



One of these techniques called "micro3Dslice" has been developed by Yxlon to empower customers to see their boards essentially in 3D without artifacts and limitations of a full computed tomography scan (Figure 4). This capability involves coordinated angular and rotational images, and software to reconstruct these images into an "HD" version of traditional x-ray imaging in a very short 1- to 3-minute scan time.

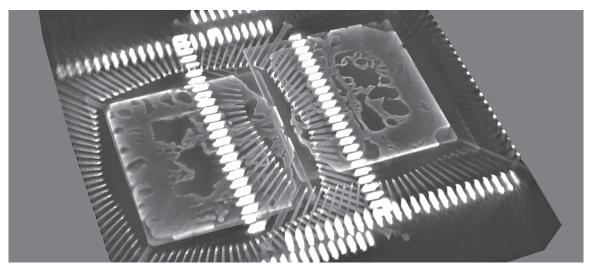


Figure 4

Void Calculation on multi-layer boards

Micro3Dslice is fast becoming one of the best ways to calculate voiding on multilayer double-sided boards, as shown in Figure 5, the two components, one on top of the board and the other on the bottom. Void calculation on these multi-layer boards is not possible in 2D. Figure 4 shows a visualization using the renderer called MAXIP (Maximum Intensity Projection).

Separating the two slices in the volume it is possible to run the void calculation for each component within a few minutes, as shown in Figure 5.

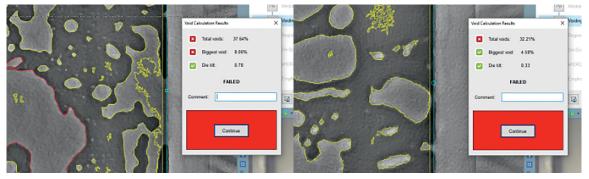


Figure 5

Determining actual fill level of THT

For through-hole technology (THT) components, calculation of the fill level seems simple per IPC, by creating a 45-degree angle view of the THT pin, then estimating total solder percent by drawing a straight line where the solder ends, if it isn't a filled barrel. However, when placing the threshold line at the limit of the visible solder joint, the angled image does not always allow accurate measurement of the solder fill. The 2D image doesn't allow determination of the actual fill level, especially if the solder wicks up the pin or the sides of the barrel. This means the measurement may fail the IPC required fill level of 75 percent - as shown in Figures 6 and 7.

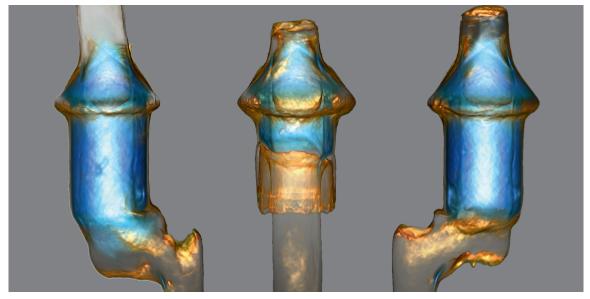


Figure 6

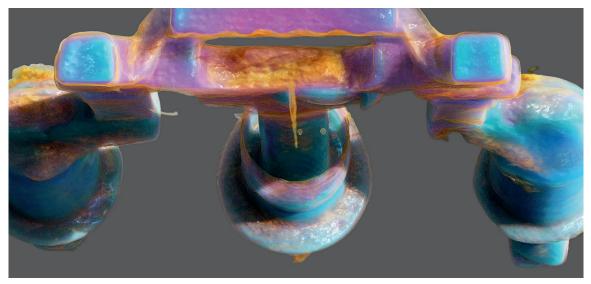


Figure 7

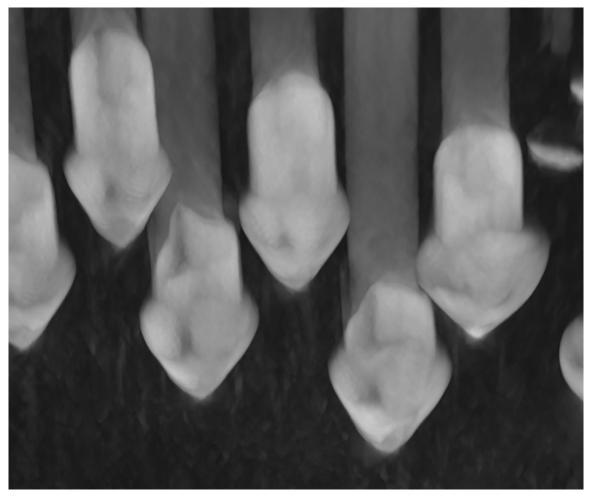


Figure 8

The solder shape in Figure 8 seems convex to the pin. This is what you can't detect in 2D and where you would set the top of the solder. However, with a small laminography volume (Figure 9) it is possible to calculate the fill level very accurately by using the volume of the solder and the air in the via, instead of manually drawing a line which is only an estimation and could be different with different users.

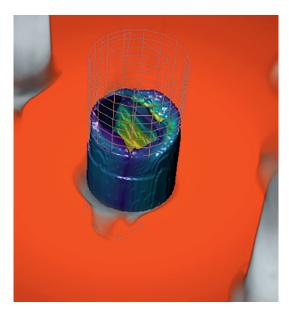


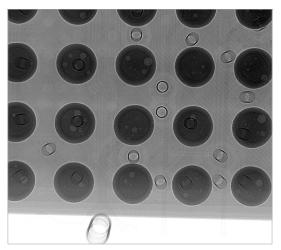
Figure 9

BGA inspection, time savings and benefits of Laminography

The advantages of using laminography for failure analysis are illustrated below in two samples.

Sample 1: Problem with a BGA

BGA failed after ICT, pin location is unknown, the 2D images make it difficult to determine the problem – especially on a multi-layer board (Figures 10 and 11).



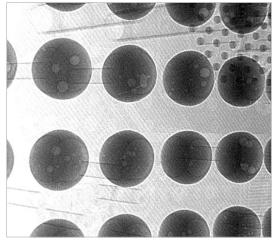


Figure 10

Figure 11

Overview of a corner of the BGA. Also with an oblique view, you can't see what could cause the failure (Figure 12).

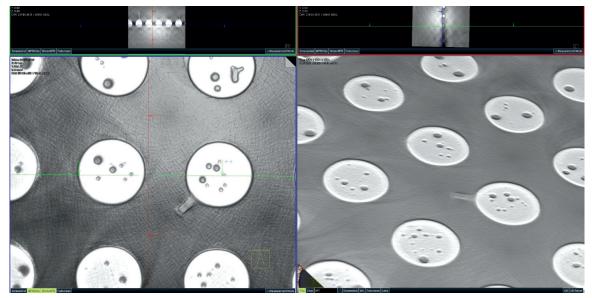


Figure 12

Laminography slice, 1 layer: Top layer with the tracks of the pad. It's clearly visible that the track is disconnected, but it isn't clear what happened (Figure 13).

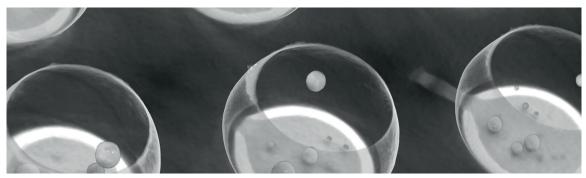


Figure 13

When you slice through the acquired laminography volume in Z, you can see that the trace is not connected (Figure 14).

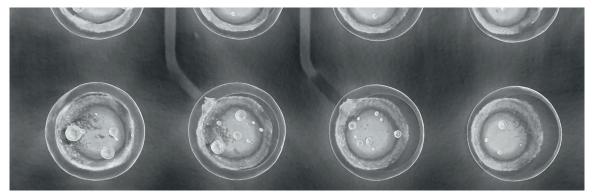


Figure 14

In another view (Figure 15), you can see that the trace is not connected but the complete pad and a small part of the trace is raised above the board.

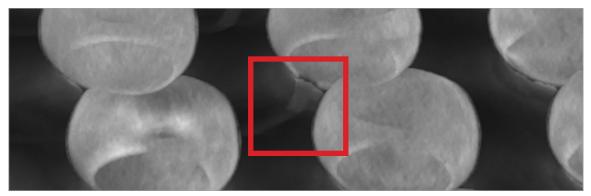


Figure 15

Limited-angle laminography is suitable for a good and quick failure analysis, when compared to CT. From many of our customer studies, we have concluded that the volume of a 2-minute micro3Dslice scan could have very comparable image quality as a 30-minute CT-Scan.

Sample 2: Problem BGA to a Connector

The problem can be located from a pin of the BGA to a connector (Figure 16).

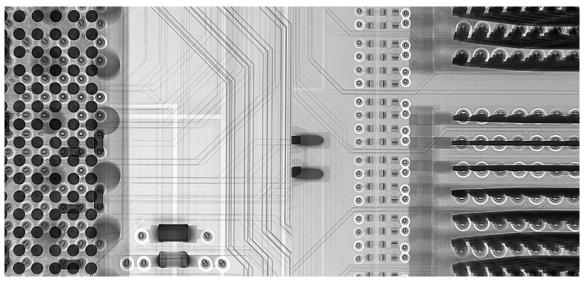


Figure 16

Once again, the problem is a multi-layer board. You can try to follow the tracks, but for a good failure analysis, you have to tilt the camera. This causes an overlapping of all components and could hide the real failure in 2D.

To make the failure analysis easier, a laminography volume was created. In this volume, you can slice from layer to layer (Figure 17).

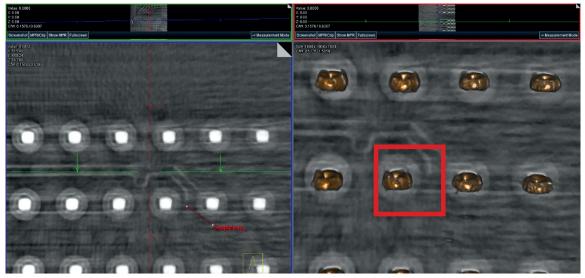


Figure 17

Track from the BGA to the connector. In Figure 18, the disconnect from the track to the pin of the connector is shown. Using the lens to highlight the failure, visualization of the pins, single layer shown in the laminography volume.

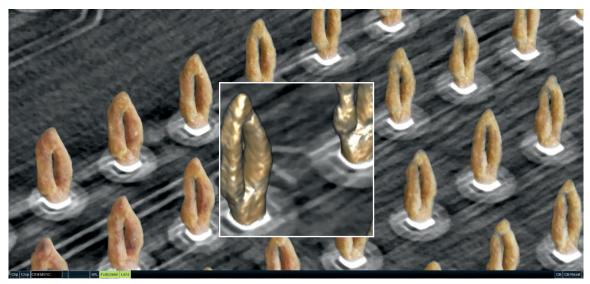


Figure 18

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With this capability we provide a tool for our customers to continue manufacturing high-quality and high-reliability products for our modern needs. To find out more about laminography and the other capabilities offered in 2D and 3D x-ray inspection technology from Yxlon, visit www.yxlon.com/en/applications/electronics.



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